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- 0912-5958431
- 0912-5958432
- 021-66717001



## 40 A standard TRIACs

### Features

- High current TRIAC
- Low thermal resistance with clip bonding
- High commutation capability
- BTA series UL1557 certified (File ref: 81734)
- Packages are RoHS (2002/95/EC) compliant

### Applications

- On/off function in static relays, heating regulation, induction motor starting circuits
- Phase control operations in light dimmers, motor speed controllers, and similar

### Description

Available in high power packages, the BTA/BTB40-41 series is suitable for general purpose AC switching.

The BTA series provides an insulated tab (rated at 2500 V rms).

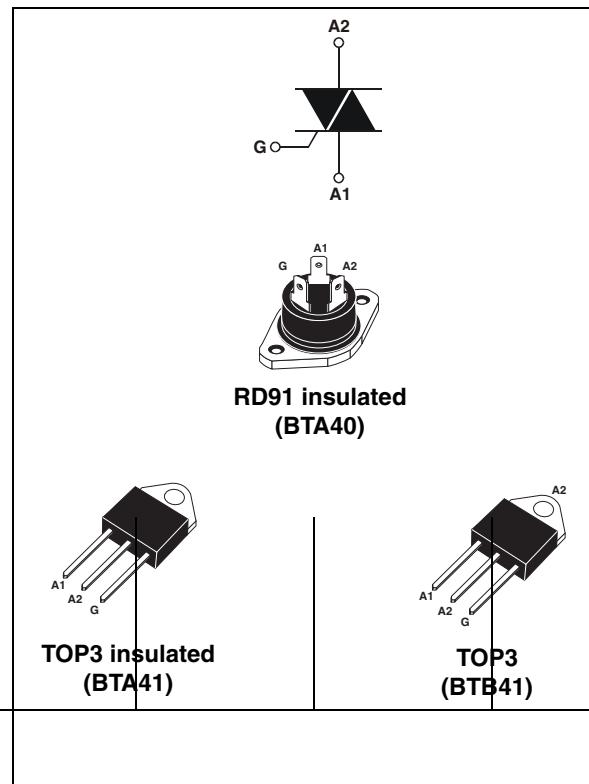


Table 1. Device summary

Symbol	Parameter	BTA40 <sup>(1)</sup>	BTA41 <sup>(1)</sup>	BTB41	Unit
I <sub>T</sub> (RMS)	On-state rms current	40	41	41	A
V <sub>DRM/V<sub>RRM</sub></sub>	Repetitive peak off-state voltage	600 and 800	600 and 800	600 and 800	V
I <sub>GT</sub>	Triggering gate current	50	50	50	mA

# 1 Characteristics

**Table 2. Absolute maximum ratings**

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	On-state rms current (full sine wave)	TOP3	$T_c = 95^\circ C$	40	A
		RD91 / TOP ins.	$T_c = 80^\circ C$		
$I_{TSM}$	Non repetitive surge peak on-state current (full cycle, $T_j$ initial = 25 °C)	F = 50 Hz	t = 20 ms	400	A
		F = 60 Hz	t = 16.7 ms	420	
$I^2t$	$I^2t$ Value for fusing	$t_p = 10 \text{ ms}$		1000	A²s
$dI/dt$	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$ , $t_r \leq 100 \text{ ns}$	F = 120 Hz	$T_j = 125^\circ C$	50	A/μs
$V_{DSM}/V_{RSM}$	Non repetitive surge peak off-state voltage	$t_p = 10 \text{ ms}$	$T_j = 25^\circ C$	$V_{DSM}/V_{RSM} + 100$	V
$I_{GM}$	Peak gate current	$t_p = 20 \mu\text{s}$	$T_j = 125^\circ C$	8	A
$P_{G(AV)}$	Average gate power dissipation		$T_j = 125^\circ C$	1	W
$T_{stg}$ $T_j$	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 125	°C

**Table 3. Electrical characteristics ( $T_j = 25^\circ C$ , unless otherwise specified)**

Symbol	Parameter			Value	Unit
$I_{GT}^{(1)}$	$V_D = 12 \text{ V}$ $R_L = 33 \Omega$	I - II - III	MAX.	50	mA
		IV		100	
$V_{GT}$		ALL	MAX.	1.3	V
$V_{GD}$	$V_D = V_{DRM}$ $R_L = 3.3 \text{ k}\Omega$ $T_j = 125^\circ C$	ALL	MIN.	0.2	V
$I_H^{(2)}$	$I_T = 500 \text{ mA}$		MAX.	80	mA
$I_L$	$I_G = 1.2 I_{GT}$	I - III - IV	MAX.	70	mA
		II		160	
$dV/dt^{(2)}$	$V_D = 67\% V_{DRM}$ gate open	$T_j = 125^\circ C$	MIN.	500	V/μs
$(dV/dt)c^{(2)}$	$(dI/dt)c = 20 \text{ A/ms}$	$T_j = 125^\circ C$	MIN.	10	V/μs

1. Minimum  $I_{GT}$  is guaranteed at 5% of  $I_{GT}$  max.

2. for both polarities of A2 referenced to A1

**Table 4. Static characteristics**

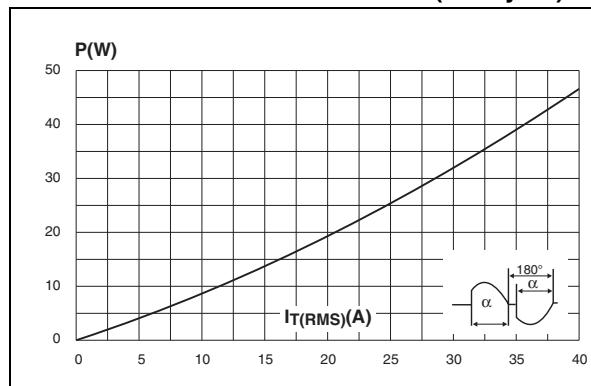
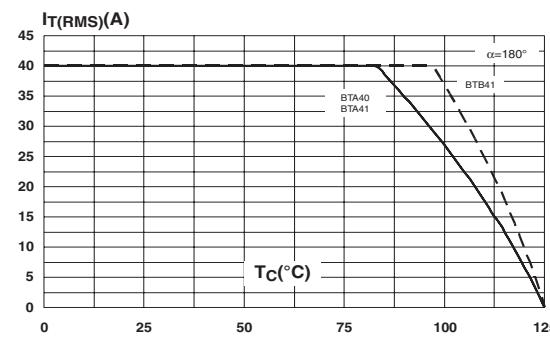
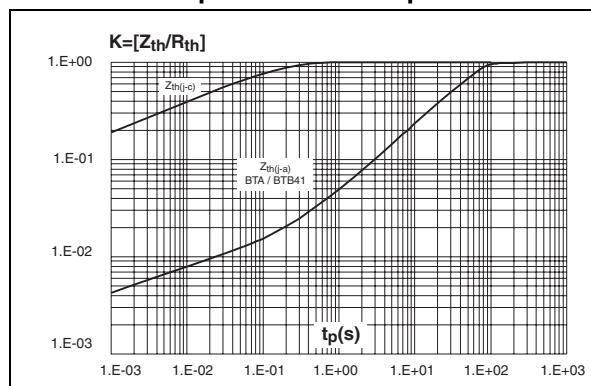
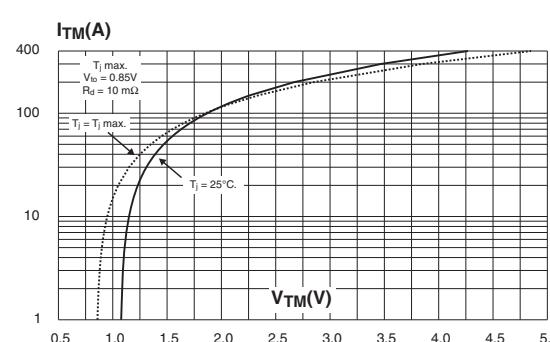
Symbol	Test conditions			Value	Unit
$V_T^{(1)}$	$I_{TM} = 60 \text{ A}$	$t_p = 380 \mu\text{s}$	$T_j = 25^\circ\text{C}$	MAX.	1.55 V
$V_{t0}^{(2)}$	Threshold voltage		$T_j = 125^\circ\text{C}$	MAX.	0.85 V
$R_d^{(2)}$	Dynamic resistance		$T_j = 125^\circ\text{C}$	MAX.	10 mΩ
$I_{DRM}$ $I_{RRM}$	$V_{DRM} = V_{RRM}$		$T_j = 25^\circ\text{C}$	MAX.	5 μA
			$T_j = 125^\circ\text{C}$		5 mA

1. Minimum  $I_{GT}$  is guaranteed at 5% of  $I_{GT}$  max.

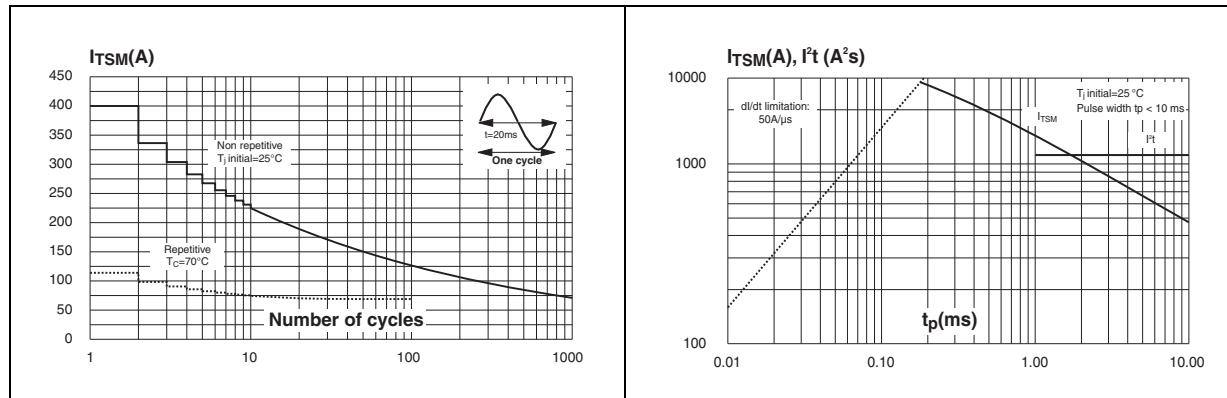
2. for both polarities of A2 referenced to A1

**Table 5. Thermal resistance**

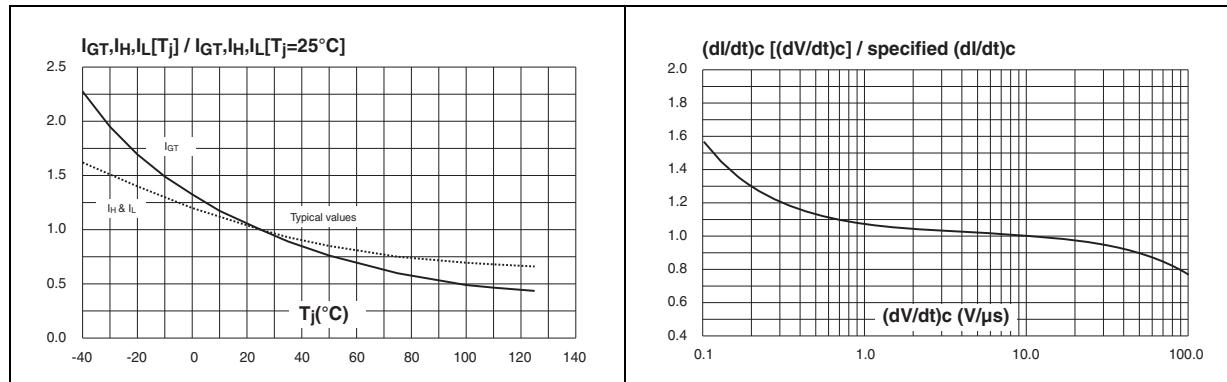
Symbol	Test conditions		Value	Unit
$R_{th(j-c)}$	Junction to case (AC)	RD91 (insulated) / TOP3 insulated	0.9	°C/W
		TOP3	0.6	
$R_{th(j-a)}$	Junction to ambient	TOP3 / TOP3 insulated	50	°C/W

**Figure 1. Maximum power dissipation versus on-state rms current (full cycle)****Figure 2. On-state rms current versus case temperature (full cycle)****Figure 3. Relative variation of thermal impedance versus pulse duration****Figure 4. On-state characteristics (maximum values)**

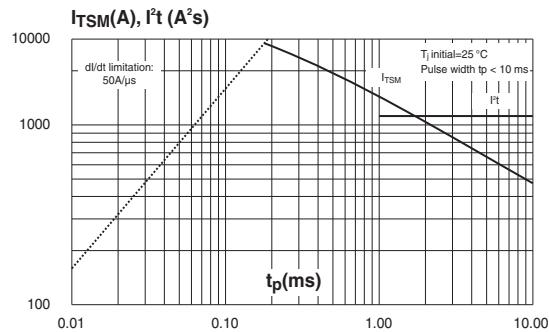
**Figure 5. Surge peak on-state current versus number of cycles**



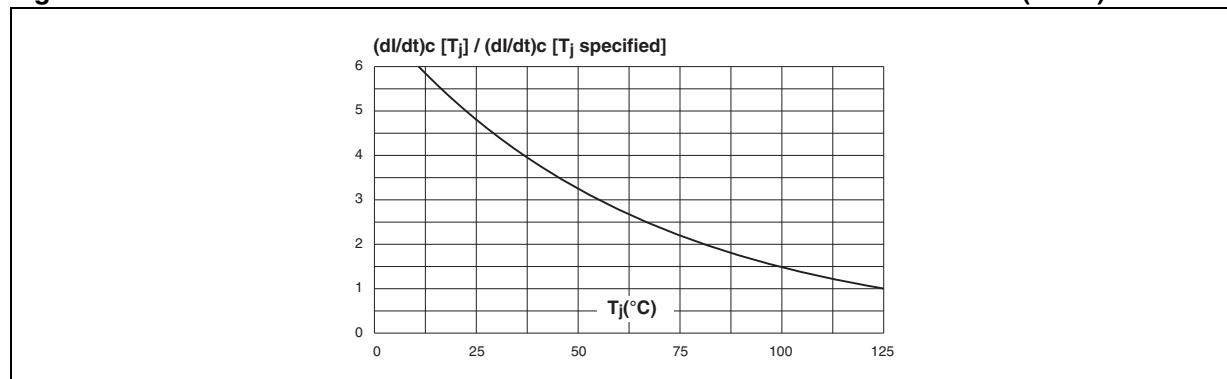
**Figure 7. Relative variation of gate trigger, holding and latching current versus junction temperature**



**Figure 6. Non-repetitive surge peak on-state current for a sinusoidal pulse and corresponding value of  $I^2t$**

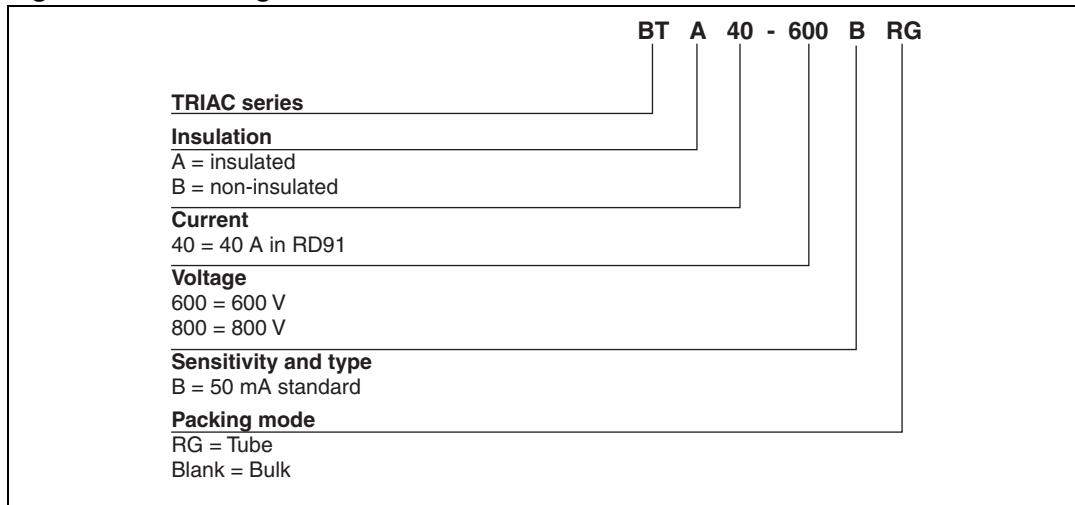


**Figure 8. Relative variation of critical rate of decrease of main current versus  $(dV/dt)c$  (typical values)**



## 2 Ordering information scheme

Figure 10. Ordering information scheme



### 3 Package information

- Epoxy meets UL94, V0
- Lead-free packages

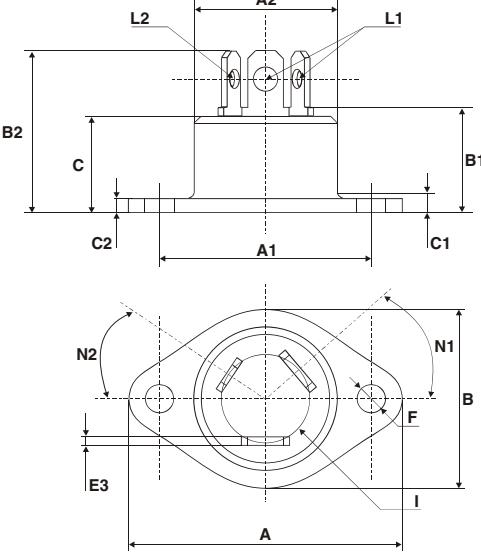
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).  
ECOPACK® is an ST trademark.

**Table 6. TOP3 insulated and non-insulated dimensions**

Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.4	4.6	0.173	0.181
B	1.45	1.55	0.057	0.061
C	14.35	15.60	0.565	0.614
D	0.5	0.7	0.020	0.028
E	2.7	2.9	0.106	0.114
F	15.8	16.5	0.622	0.650
G	20.4	21.1	0.815	0.831
H	15.1	15.5	0.594	0.610
J	5.4	5.65	0.213	0.222
K	3.4	3.65	0.134	0.144
ØL	4.08	4.17	0.161	0.164
P	1.20	1.40	0.047	0.055
R	4.60 typ.		0.181 typ.	

Table 7. RD91 dimensions

Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	-	40.00	-	1.575
A1	29.90	30.30	1.177	1.193
A2	-	22.00	-	0.867
B	-	27.00	-	1.063
B1	13.50	16.50	0.531	0.650
B2	-	24.00	-	0.945
C	-	14.00	-	0.551
C1	-	3.50	-	0.138
C2	1.95	3.00	0.077	0.118
E3	0.70	0.90	0.027	0.035
F	4.00	4.50	0.157	0.177
I	11.20	13.60	0.441	0.535
L1	3.10	3.50	0.122	0.138
L2	1.70	1.90	0.067	0.075
N1	33°	43°	33°	43°
N2	28°	38°	28°	38°



The technical drawing illustrates the RD91 package in two views: a top view showing the lead frame and bond wires, and a bottom view showing the chip and bond pads. Key dimensions labeled include: A (total width), A1 (width of the chip area), A2 (width of the bond pads), B (total height), B1 (height of the chip area), B2 (height of the bond pads), C (width of the lead frame), C1 (width of the lead frame at the base), C2 (width of the lead frame at the top), E3 (width of the lead frame at the base), F (width of the lead frame at the top), I (length of the lead frame), L1 (width of the lead frame at the top), L2 (width of the lead frame at the base), N1 (angle of the lead frame at the top), and N2 (angle of the lead frame at the base). The top view also shows bond wires labeled L1 and L2 extending from the bond pads.

## 4 Ordering information

**Table 8. Ordering information**

Order code <sup>(1)</sup>	Marking	Package	Weight	Base qty	Delivery mode
BTA40-xxxB	BTA40xxxB	RD91	20 g	25	Bulk
BTA41-xxxBRG	BTA41xxxB	TOP3 Ins.	4.5 g	30	Tube
BTB41-xxxBRG	BTB41xxxB	TOP3	4.5 g	30	Tube

1. xxx = voltage

## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
Sep-2003	5	Last update.
25-Mar-2005	6	TOP3 delivery mode changed from bulk to tube.
14-Oct-2005	7	T <sub>c</sub> values for I <sub>T</sub> changed in Table 3. ECOPACK statement added.
10-Aug-2009	8	Updated <a href="#">Table 2</a> to correctly place packages. Updated <a href="#">Figure 2</a> . <a href="#">Table 5</a> changed to correctly place TOP3. Updated ECOPACK statement.